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Term	Documents
(7 AND 23).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	44
(L23 AND L7).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	44

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L27

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<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L27</u>	L23 and l7	44	<u>L27</u>
<u>L26</u>	L23 and l6	4	<u>L26</u>
<u>L25</u>	L23 and l5	280	<u>L25</u>
<u>L24</u>	L23 and l4	166	<u>L24</u>
<u>L23</u>	L22 and l1	1269	<u>L23</u>
<u>L22</u>	(conflict\$3 or contention\$1 or contend\$3 or hazard\$5) near15 read\$3 near15 writ\$4	2422	<u>L22</u>
<u>L21</u>	L17 and l7	0	<u>L21</u>
<u>L20</u>	L17 and l6	0	<u>L20</u>
<u>L19</u>	L17 and l5	4	<u>L19</u>
<u>L18</u>	L17 and l4	7	<u>L18</u>
<u>L17</u>	L16 and read\$3 near15 writ\$3 near15 interlock\$4	24	<u>L17</u>

L16 (recover\$7 or resum\$6) near8 address\$3

7088 L16

*DB=PGPB,USPT; PLUR=YES; OP=OR*

L15 l2 and l7

4 L15

L14 l2 and l6

1 L14

L13 l2 and l5

30 L13

L12 l2 and l4

32 L12

L11 l3 and l7

2 L11

L10 l3 and l6

0 L10

L9 l3 and l5

20 L9

L8 l3 and l4

19 L8

L7 (712/216,217)[CCLS]

823 L7

L6 (711/155)[CCLS]

182 L6

L5 (711/140-221)![CCLS]

17320 L5

L4 (712/2-300)[CCLS]

10993 L4

*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L3 L2 and (recover\$7 or resum\$6)

95 L3

L2 L1 and read\$3 near15 writ\$3 near15 interlock\$4

191 L2

L1 (writ\$5 or read\$6) near5 (queue\$3 or buffer\$4)

96956 L1

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IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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- |                          |   |
|--------------------------|---|
| <input type="checkbox"/> | <p><b>1. Register locking in an asynchronous microprocessor</b><br/> Paver, N.C.; Day, P.; Furber, S.B.; Garside, J.D.; Woods, J.V.;<br/> Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings., IEEE 1992 International<br/> 11-14 Oct. 1992 Page(s):351 - 355<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDE</a>(356 KB) IEEE CNF</p>                               |
| <input type="checkbox"/> | <p><b>2. Relating buffer-oriented microarchitecture validation to high-level pipeline functionality</b><br/> Utamaphethai, N.; Blanton, R.D.; Shen, J.P.;<br/> High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IEEE International<br/> 7-9 Nov. 2001 Page(s):3 - 8<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDE</a>(218 KB) IEEE CNF</p>                             |
| <input type="checkbox"/> | <p><b>3. Design considerations and implementations of a high performance dynamic register file</b><br/> Joshi, R.V.; Hwang, W.;<br/> VLSI Design, 1999. Proceedings. Twelfth International Conference On<br/> 7-10 Jan. 1999 Page(s):526 - 531<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDE</a>(984 KB) IEEE CNF</p>  |
| <input type="checkbox"/> | <p><b>4. Performance analysis of the ATLAS Second-Level Trigger software</b><br/> Bogaerts, J.A.C.; Botterill, D.R.; Weidong Li; Middleton, R.P.; Werner, P.; Wickens, R.J.; Zobemig, H.;<br/> Nuclear Science, IEEE Transactions on<br/> Volume 49, Issue 2, April 2002 Page(s):383 - 388<br/> <a href="#">AbstractPlus</a>   <a href="#">References</a>   Full Text: <a href="#">PDE</a>(255 KB) IEEE JNL</p> |
| <input type="checkbox"/> | <p><b>5. A personal computer-based monitoring and control system for electron accelerators</b><br/> Van Ausdela, L.A.; Haskell, K.J.; Jones, J.L.;<br/> Particle Accelerator Conference, 2001. PAC 2001. Proceedings of the 2001<br/> Volume 2, 18-22 June 2001 Page(s):828 - 830 vol.2<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDE</a>(549 KB) IEEE CNF</p>                                 |


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